CLAIMS

1. An apparatus for determining convergence of an equalizer (20), comprising:

an equalizer (28) output signal;

a nearest element decision device (29), the nearest element decision device (29) receiving the equalizer (28) output signal and creating a decision device (29) output signal containing permissible symbol values; and

a monitoring circuit (31), the monitoring circuit (31) receiving the decision device (29) output signal and applying a test criterion to data contained in the decision device (29) output signal so as to determine equalizer (28) convergence.

2. The apparatus of claim 1, wherein the equalizer (28) is formed to include an infinite impulse response filter.

3. The apparatus of claim 1, wherein the nearest element decision device (29) is a slicer.

4. The apparatus of claim 1, wherein the monitoring circuit (31) receives the decision device (29) output signal for a predetermined period of time representing an acquisition of a desired number of transmitted symbol values.

5. The apparatus of claim 4, further comprising a memory, the memory being coupled to the monitoring circuit (31) and being adapted to store decision device (29) output data and test criteria.

6. The apparatus of claim 5, wherein the test criteria for determining equalizer (28) convergence includes identifying a desired sample of transmitted symbol values.

7. The apparatus of claim 6, wherein the desired sample of transmitted symbol values includes at least one of every possible symbol value.

8. The apparatus of claim 1, wherein the monitoring circuit (31) is coupled to the equalizer (28), the monitoring circuit (31) resetting the equalizer (28) when the equalizer (28) diverges.

9. The apparatus of claim 1, wherein the monitoring circuit (31) is coupled to the equalizer (28), the monitoring circuit (31) resetting the equalizer (28) when the equalizer (28) achieves an invalid state.

10. The apparatus of claim 1, wherein the equalizer (28) output signal includes an image representative datastream containing data packets.

11. The apparatus of claim 1, wherein the monitoring circuit (31) is a microprocessor.

12. An equalizer status monitoring device for use in a digital communication system, the device including an adaptive channel equalizer (28), a slicer (29) and a monitoring circuit (31), wherein the digital communications system receives a vestigial sideband modulated signal containing high definition video information represented by a multiple level symbol constellation, the data having a data frame format constituted by a succession of data frames, the adaptive channel equalizer (28) generating a first output signal which is input to the slicer (29), the slicer (29) generating a second output signal which is input to the monitoring circuit (31), the

monitoring circuit (31) applying a test criteria to the second output signal to determine convergence of the adaptive channel equalizer (28).

13. The system of claim 12, wherein the monitoring circuit (31) is coupled to the adaptive channel equalizer (28) and resets the adaptive channel equalizer (28) when the adaptive channel equalizer (28) diverges.

14. The system of claim 12, wherein the monitoring circuit (31) is coupled to the adaptive channel equalizer (28) and resets the adaptive channel equalizer (28) when the adaptive channel equalizer (28) assumes an invalid state.

15. The system of claim 12, wherein the test criteria for determining convergence requires identifying at least some transmitted symbol values.

16. The system of claim 12, wherein the adaptive channel equalizer (28) further comprises an infinite impulse response filter.

17. The system of claim 12, wherein the test criteria for determining convergence requires identifying at least one of each possible transmitted symbol value.

18. The system of claim 12 wherein the monitoring circuit (31) is a microprocessor.

19. In a digital communications receiver including an adaptive equalization filter (28) that desirably achieves a state of convergence and which undesirably achieves a state of divergence or an invalid state, a method of monitoring the state of the equalization filter (28) comprising the steps of:

coupling an output signal from the equalization filter (28) to a monitoring circuit (31);

causing the monitoring circuit (31) to examine data contained within the output signal for a finite time period;

causing the monitoring circuit (31) to apply a test protocol to the examined data; and

causing the monitoring circuit (31) to reset the equalization filter (28) when the test protocol detects a state of divergence.

20. A method according to claim 19, further comprising the step of causing the monitoring circuit (31) to reset the equalization filter (28) when the test protocol detects that the equalization filter (28) has achieved an invalid state.

21. A method according to claim 19, further comprising the steps of:

coupling the equalization filter (28) output signal to a slicer (29); and

coupling the slicer (29) to the monitoring circuit (31) such that the monitoring circuit (31) examines data generated by the slicer (29).

22. A method according to claim 21, wherein the test protocol requires detection of each possible transmitted symbol value within the data generated by the slicer (29) in order to find that the equalization filter (28) has achieved a state of convergence.

23. The method of claim 19 wherein the monitoring circuit (31) is a microprocessor.